International Journal of ChemTech Research
CODEN (USA): IJCRGG ISSN: 0974-4290
Vol.7, No.2, pp 1014-1018, 2014-2015

ICONN 2015 [4th - 6th Feb 2015]
International Conference on Nanoscience and Nanotechnology-2015
SRM University, Chennai, India

Simulation Analysis of Conduction In Ultra Thin Nano Scale Fully Depleted SOI MOSFET

Prashantmani[1]* and Manoj Kumar Pandey[1]

[1]SRM University NCR Campus, Ghaziabad, India.

Abstract : The present paper is about the simulation analysis of conduction in Ultra Thin Nano Scale Fully Depleted Silicon On Insulator MOSFET (UTN MOSFET).The low power application attracts the threshold voltage scale down .The physical dimension of the device requires more attention to scale down as size reaches to nano range. The device having thin silicon layer above BOX(buried Oxide) i.e. T_{si}=15 nm and T_{ox}=3nm results the threshold voltage of the device reduced . The short channel effect (SCE) is reduced as lateral direction engineering implemented in device. DIBL and Subthreshold rolloff is also considered . The analysis of Kink effect is also considered and we find the device is virtually free of kink.
Keywords: SOI MOSFET, Scaling , Ultra Thin MOSFET's, Kink Effect

Introduction

Now days the scaling is most interesting part of modern device design engineering due to reduction in chip size. Industry demand for improved performance, scaling of SOI MOSFET's has reached the regime of short channel for improved speed , narrow width for lower power consumption and ultra thin silicon film layer for reducing the short channel effects. Silicon - On - Insulator (SOI) devices are a relatively widely used technology. Although the technology has been used around since the 1960‟s, SOI devices are only recently becoming commercially viable, due to the cost associated in producing the devices[1-3]. SOI devices are an advancement of standard MOSFET technology. The difference between SOI and MOSFET technology is the inclusion of an insulating layer. SOI MOSFET's are created from a thin layer of silicon placed on top of insulating layer. SOI MOSFET's performance advantage over conventional bulk MOSFET's is mainly from lower average threshold-voltage due to transient floating-body (FB) operation and lower junction capacitance[4-6]. The partial depleted (PD) instead of fully depleted (FD) SOI has become the desirable choice for mainstream digital applications, due to the simple of manufacturing, better control of short channel effects, larger design window for the threshold voltage, and lower self-heating effect[7].

The cross sectional view of UTN-MOSFET is Figure 1 .The Ultra Thin fully depleted SOI MOSFET is terminology used where the silicon film thickness T_{si} is thin layer in range of below 30-50 nm. In our device the thickness of gate oxide T_{OX} is range of 3 nm and T_{si} is 30 nm . The buried oxide thickness is 50 nm and the source and drain thickness is 30 nm .The width of the channel is 25 nm as we know the ratio of Width and Length should be less than one .The doping profile in the channel is 3×10^{18} cm^{-3} and the doping profile of source and drain is 1×10^{20} cm^{-3}.The Threshold voltage of the device vary as the T_{si} is thinner so the device will

be more usefull in low power application. The other parameter like Subthreshold voltage and Leakage current will be reduced as scaling done in $T_{si.}$ Because of the elimination of the coupling of source-substrate and drain-substrate the suppression of short channel effects occur in device.

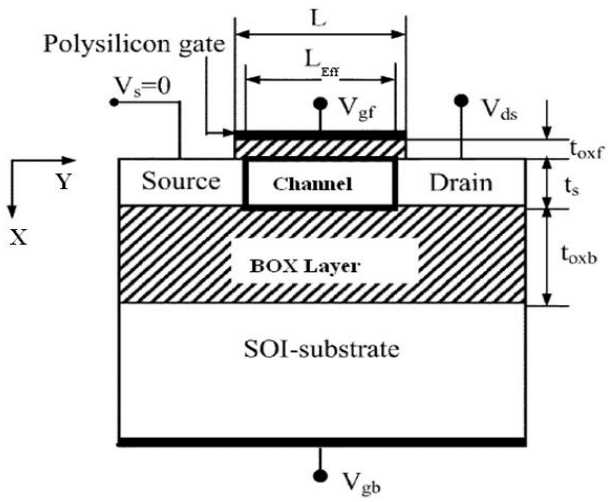

Figure 1: Cross-sectional view of UTNFD-SOI-MOSFET

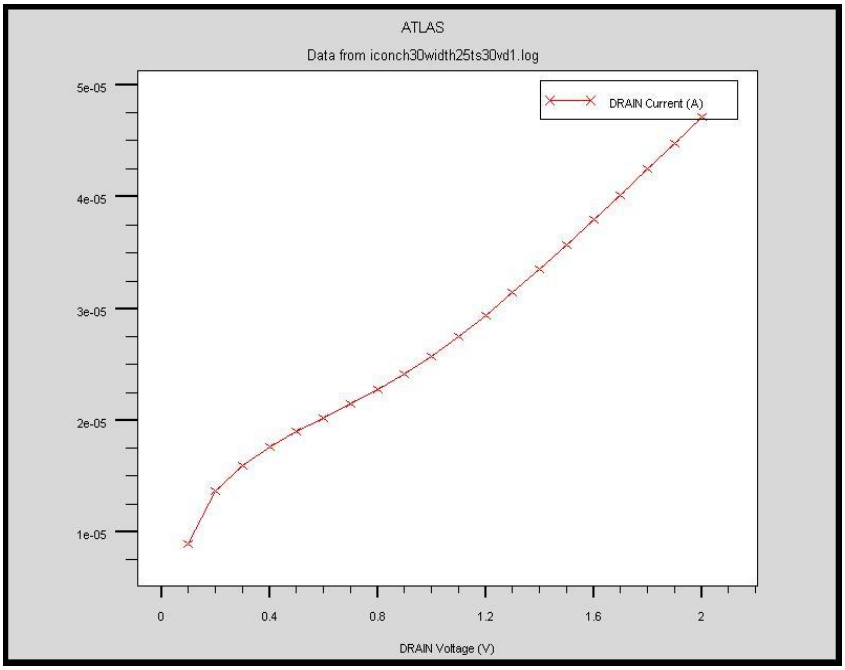

Figure2: I_d-V_d curve for the Ultra Thin Nano scale FD MOSFET for V_{gs}=1.0 V and T_{si}=30 nm and N_A=3×10^{18} cm^{-3} .

Result & Discussion

From Figure 2 we observed the drain current and drain voltage of the device at Gate source voltage 1.0 volt. Where applied gate source voltage (Vgs) is 1.0 Volt, the thickness of the silicon film (T_{si}) is 30 nm and the thickness of the oxide layer (T_{ox}) is 3nm. The doping profile in the channel is 3×10^{18} cm^{-3} and doping profile in source and drain is 1×10^{20} cm^{-3}. By observation of the Figure 2 we came to the conclusion that the device is virtually free of kink effect.

The MOSFET's Transconductance curve is shown by Figure 3 at V_{ds}=1.0 volt and thickness of the silicon film is 30 nm ,thickness of the oxide is 3 nm . The doping profile in the channel is N_A=3×10^{18} cm^{-3}and the doping in the source and drain is 1×10^{18}cm^{-3}.The drain current is increased as the gate voltage increased and we observed the threshold voltage of the device is 0.2 Volt.

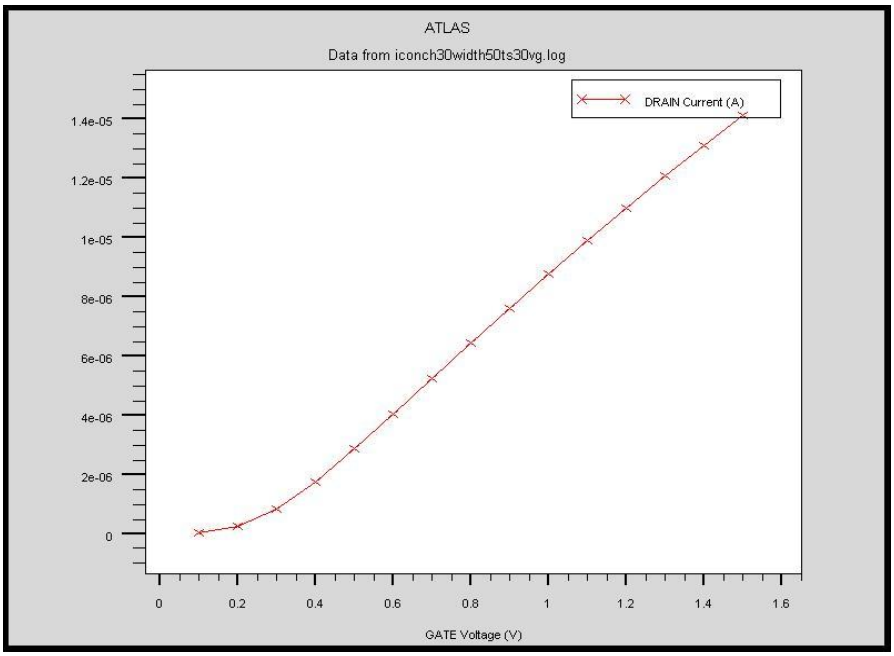

Figure3: I_d-V_g curve for the Ultra Thin Nano scale FD MOSFET for V_{ds}=1.0V and T_{si}=30 nm and N_A=3×10^{18} cm^{-3} .

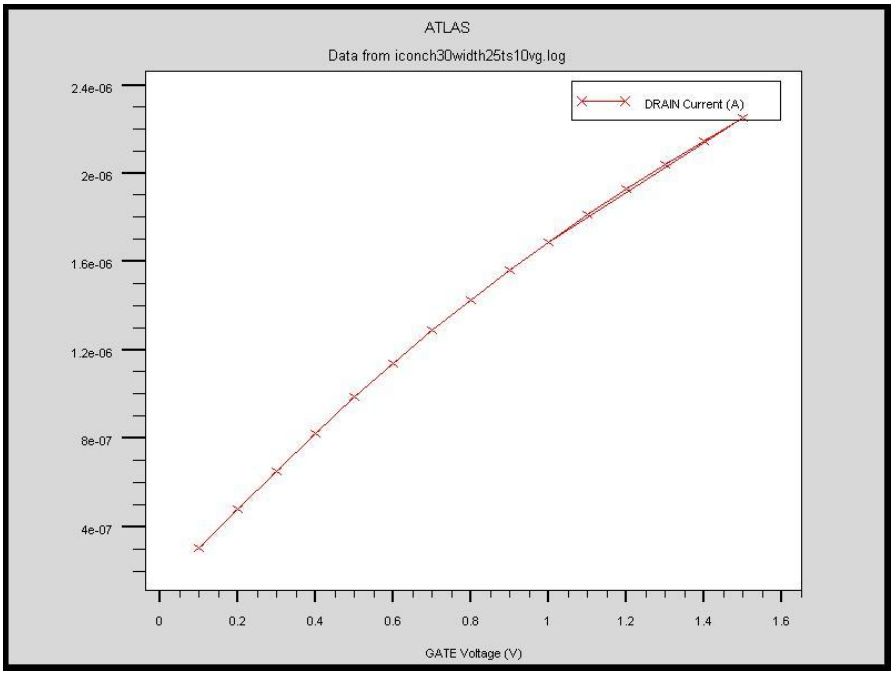

Figure4 :I_d-V_g curve for the Ultra Thin Nano scale FD MOSFET for V_{ds}=0.10V and T_{si}=15 nm and N_A=3×18 cm^{-3} .

The MOSFET's drain current and drain source characterstic is shown by Figure 3 at V_{ds}=0.10 volt and thickness of the silicon film (T_{si}) is 15 nm, thickness of oxide (Tox)is 3 nm . The doping profile in the channel is N_A=3×18 cm^{-3}.The drain current is increased as the gate voltage increased and we observed the threshold voltage of the device is 0.17485 Volt. So we can say the threshold voltage is reduced as we reduce the thickness of silicon film T_{si}. We also analyze the effect of the channel width with various electrical parameters. From Figure 5-6 the characteristics at width of the channel is W=15 nm and W=20nm the threshold voltage is 0.199194V and 0.2 V. i.e. Narrow Width Effect observed in UTN- MOSFET. The structure of the device is given in Table 1 and the electrical properties of the device is give in Table 2, which shows the Narrow Width Effect . The effect of variation in T_{si} is given in Table3.

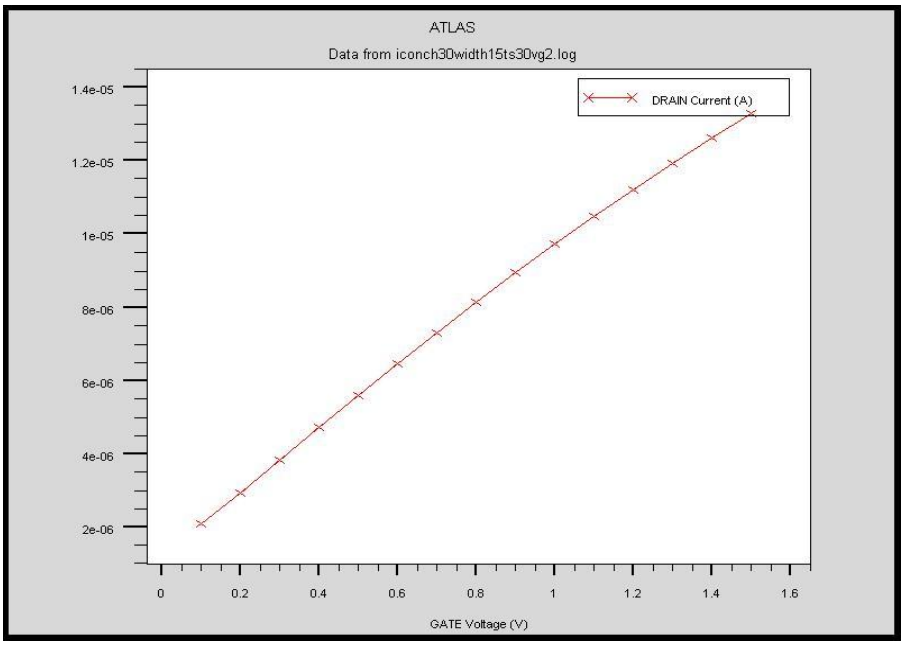

Figure5: I_d-V_g curve for the Ultra Thin Nano scale FD MOSFET for width of channel W=15nm V_{ds}=0.10V and T_{si}=30 nm and N_A=3×18 cm^{-3} .

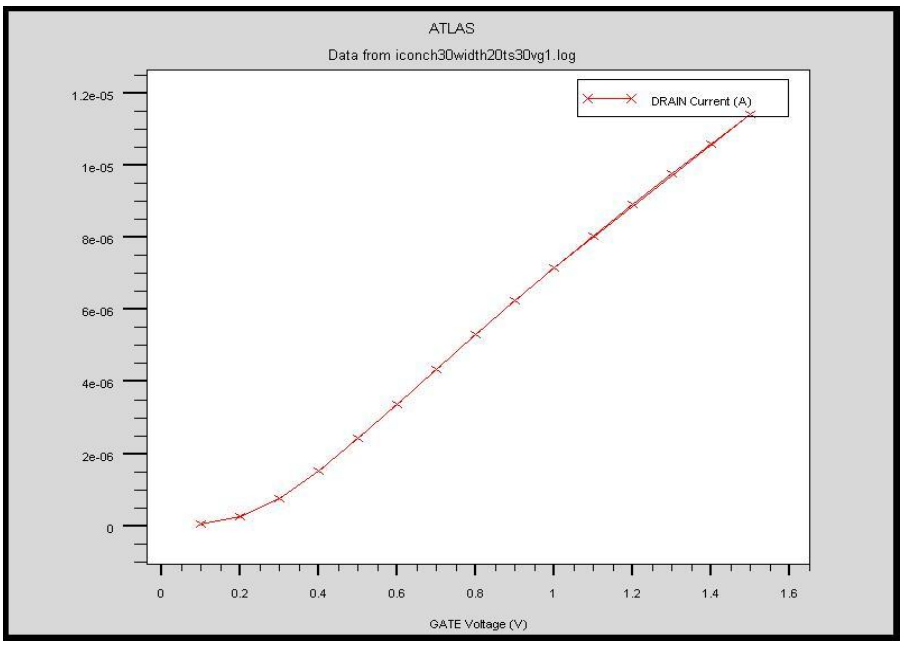

Figure6: I_d-V_g curve for the Ultra Thin Nano scale FD MOSFET for width of channel W =20nmV_{ds}=1.0V and T_{si}=30 nm and N_A=3×18 cm^{-3} .

Table 1: Device Structure Parametrs of UTN-MOSFET

Device Structure Parameters	**UTN -MOSFET**
Channel Length(L)	30 nm
Gate Length	30nm
Thickness of Silicon Film	15nm,30nm,40nm
Thickness of Gate Oxide	3nm
Channel Doping Profile	3×18cm^{-3}

Table 2:Device Electrical Properties of UTN-MOSFET

Electrical Properties	**At Width (15nm)**	**Width(20nm)**	**Width(30nm)**
Vth(V)	0.199194 V	0.2V	0.27346V
Sub Vth(V)	0.150772V/decade	0.145958 V/decade	0.12578V/decade
Ids Leakage current(A/μm)	3.75105e-005 A/μm	4.71405e-005 A/μm	1.71057e-005 A/μm

Table 3:.Device Electrical Properties of UTN-MOSFET

Electrical Properties	T_{si}=30nm	T_{si}=15nm	T_{si}=40nm
Vth (V)	0.199194V	0.17485V	0.201963V

Conclusion

The developed SOI n-MOSFET structure using process simulator Silvaco-ATLAS is observed for the various electrical properties. As observed the device n- MOSFET structure with SOI shows the improved electrical characteristics and when scaling continues in the Narrow width effects will also appear reduced the leakage current and sub threshold conduction. In other prospect thin silicon film FD MOSFETs are useful in low power application.

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